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Throughout the period of AFOSR support we concetrated on research on hardware design, operating system support, mathematical software design, and applications programming for concurrent computing systems. Multiple Instruction Multiple Data computing systems constituted the focus of our attention at the hardware and software levels. At every stage we used hardware that conformed absolutely to the IEEE Standard for Binary Floating Point Arithmetic, P754, IEEE Computer Society.

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FINAL TECHNICAL REPORT; "CONCURRENT COMPUTING: NUMERICAL

ALGORITHMS and SOME APPLICATIONS," AFOSR Grant #82-0210

Submitted by Virginia C. Klema, Principal Investigator

and Project Manager, January 23, 1990.

Throughout the period of AFOSR support we concentrated on
research on hardware design, operating system support,
mathematical software design, and applications programming
for concurrent computing systems. Multiple Instruction
Multiple Data computing systems constituted the focus of
our attention at the hardware and software levels. At
every stage we used hardware that conformed absolutely to
the IEEE Standard for Binary Floating Point Arithmetic,
P754, IEEE Computer Society.

At first, the hardware that we used was especially constructed
seven-processor systems using Intel multi-function boards
with the IEEE Standard in hardware on a chip. With these
low level systems (the only ones that could be used at the
time) we concentrated on minimal operating systems to support
concurrent computing applications and built certain utilities
to assist debugging operations. The lack of debugging support
constituted a major hurdle for research on mathematical
software for concurrent computing applications.

Later on, when concurrent computing systems became available
from vendors, we moved our research to two specific systems:
the Intel 32 node iPSC, and the BBN Butterfly. These are
two distinctly different hardware designs. We were aware
that hardware designs were certain to change over time, and

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thus research should not be parochial to the design of any
particular machine. Until yet it is not possible to achieve
portability of applications across different hardware designs.
However highly modular operating systems and numerical soft-
ware greatly assist such portability. In particular, by
creating a message passing system for the BBN Butterfly we
were able to port applications from the Intel iPSC to and
from the BBN Butterfly.

Throughout the period of research we divided the applications
among the processing elements. We did not segment any specific
algorithms, for example, solution of linear systems or eigen
systems. Such segmentation would be useful on computing
systems that have very small granularity, say, Single
Instruction Multiple Data machines such as the Thinking
Machines Connection Machine.

Our applications consisted of, but were not limited to,
statistical computations of least squares fits aimed at
determining influential observations, and iteratively re-
weighted least squares. These and many other statistical
computations have inherent parallelism that can be exploited
without degradation of the expected speed-up on concurrent
systems.

MIT graduate students and undergraduate research assistants
were supported by this research. Senior personnel included
Elizabeth Ducot who supervised the operating system support
group. Patrick Barton supervised hardware configuration
and system implementation. The principal investigator
supervised the mathematical software and the applications.